REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated November 19, 2003. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-14 are under consideration in this application. Claims 1-14 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicants' invention.

Additional Amendments

The claims are being amended to correct formal errors and/or to better disclose or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

Figures 9A-9D were objected to and should be designated with a legend "Prior Art". Claims 1-14 were objected for minor informalities. Claims 4-8 and 12-14 were rejected under 35 U.S.C. § 112, second paragraph, on the grounds of being vague and indefinite. As indicated, the claims and drawings have been amended as required by the Examiner. Accordingly, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Prior Art Rejections

Claims 1, 4, 5 and 9 were rejected under 35 U.S.C. § 102(b) on the grounds of being anticipated by US Pat. No. 5,715,476 to Kundu et al. (hereinafter "Kundu"). Claims 2, 6, 7, 10, 12, and 13 were rejected under 35 U.S.C. § 103(a) on the grounds of being anticipated by Kundu in view of US Pat. No. 6,081,853 to Gaskins et al. (hereinafter "Gaskins"), and against claims

3, 8, 11 and 14 as being unpatentable over Kundu in view of Gaskins and further in view of US Pat. No. 5,394,528 to Kobayashi et al. (hereinafter "Kobayashi"). The prior art references of Strongin et al. (6,185,637), Ryan (6,405,280) and Shaw (6,574,707) were cited as being pertinent to the present application. These rejections have been carefully considered, but are most respectfully traversed.

The data processing device 1 of the invention (E.g., Fig. 1), as now recited in claim 1, comprises: a cache memory 4 comprising a plurality of cache lines; a cache control part 5 for controlling the cache memory 4; and a memory control part 6 accessible to an external memory 2 (e.g., synchronous DRAM) in response to a cache mishit of the cache memory 4. In access to the external memory 2 burstable in response to a cache mishit, the memory control part 6 forms first information (e.g., WRPA) indicating a burst length of the external memory 2 and a starting address of at least one burst operation of the burst length and controls said burst operation necessary to join (p. 11, line 13) data retrieved from the starting address into a data entity with a length meeting with one cache line length of one of the cache lines (e.g., wraparounding 8 data blocks of 32 bits into a data entity in one burst transmission to store/fill in a cache line of 32 bits long, or wraparounding 4 data blocks of 16 bits into two data entities in two burst transmissions joined into one data entity to store/fill in a cache line of 32 bits long). The cache control part 6 controls a cache fill operation of filling data joined in said burst operation into the cache memory by arranging the data in order of addresses according to the first information to corresponding locations in said one of the cache lines independently whether the starting address is a top address of said one of the cache lines or not (Fig. 8 shows, for example, corresponding data D1 is always filled into cache fill address N + 0 regardless of the starting address (i.e., effective address) is N + 0, N+ 8, N+ 16, or N + 24).

The invention is also directed to a data processing system comprising a data processing device having a CPU and a cache memory; and a memory (claim 4) or a plurality of memories (claim 5) connected to the data processing device and burstable and configuring a main memory for the cache memory. The data processing device performs the same operation as the data processing device recited in claim 1. The invention is also directed to a data processing system (claim 9) comprising the data processing device recited in claim 1, a CPU accessing the cache memory, and the burstable memory.

When the processing unit tries to access the first address but the data of the first address is in the burstable memory 2, the processing unit issues a cache mishit and accesses to the burstable memory 2 to fetch the data of the first address. The processing unit requests to burst-

access the burstable memory 2 for the data of the first address, and then the burstable memory 2 outputs the data of the first address and the other data by the burst transferring. The processing unit stores data received from the memory to the cache memory. The processing unit controls storing data of the first address at a location in the cache memory to be the same whether the staring address in the cache memory is a top location of the cache line or not. The invention uses "*the cache fill address generating circuit 42 to sort the cache fill addresses* (p. 30, lines 18-23)" *during* the cache fill operation in order of wraparound by the rule of the generation logic shown in Fig. 4 for the subsequent access addresses.

For example, if the location of the starting address of the first address happens to be the same as the address of the top location N+0 of a cache line in the cache memory (e.g., the N+0 row of Fig. 8), the processing unit stores address data D1 of the top location of the cache line to the top location N+0 in the cache line, and stores address data of the second location in the cache line to the second location N+4. On the other hands, even if the location of the starting address of the first address is the address of the second location N+4 in the cache line (i.e., different from the address of the top location of the cache line N+0), the processing unit still stores the address data D2 of the second location in the cache line to the second location N+4 in the cache line, and stores the address data of the top location of the cache line to the top location N+0.

Applicants respectfully contend that none of cited prior art references teaches or suggests a data processing device "arranges the data entity joined by at least one burst transfers in order of addresses according to the first information to corresponding locations in said one of the cache lines independently whether the starting address is a top address of said one of the cache lines or not."

Kandu and Gaskins merely disclose a processing unit comprising a cache memory. The processing unit stores data to the cache memory when the cache mishit occurs and the address of the cache mishit occurring is not the same as the address of the top location in one cache line in the cache memory, and the memory performs the burst transferring with the starting address being the occurring address of cache mishit. However, they fail to disclose that the processing unit "stores/fills data in order of addresses according to the first information to corresponding locations in said one of the cache lines independently whether the starting address is a top address of said one of the cache lines or not".

Kobayashi fails to compensate for the deficiencies of Kandu and Gaskins. Kobayashi only discloses an aligner for changing the data alignment as the first prior art technique described in the specification (p. 6, 2nd paragraph; p. 31, lines 9-13; (C) in Fig. 9) with many penalty cycles, but it does not discloses "stores/fills data in order of addresses according to the first information to corresponding locations in said one of the cache lines independently whether the starting address is a top address of said one of the cache lines or not". Rather than sorting by a cache fill address generating circuit 42 (Fig. 7) "*the cache fill addresses in order of N+8, N+12, N, N+4, N+16, N+20, N+24, and N+28* (p. 30, lines 18-23)" into a linear order N, N +4, N+16, N+8, N+12, N+20, N+24, and N+28 ***during*** the cache fill operation as the invention, the "*data aligner for conforming the data order to the data order in burst operations ... is provided* ***before cache fill*** *so as not to perform cache fill with this mismatch. four penalty cycles in data sorting are generated, as shown in (C) in Fig. 9, and thus the bus performance is deteriorated* (p. 31, lines 10-13)"

Applicants contend that neither Kandu, nor Gaskins or Kobayashi teaches or discloses each and every feature of the present invention as disclosed in at least independent claims 1, 4, 5 and 9. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of

the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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